WHAT IS CLAIMED IS:

1. A mask for manufacturing integrated circuits, the mask comprising:

a mask substrate;

an active mask region within a first portion of the mask substrate, the active region being adapted to accumulate a pre-determined level of static electricity;

a first guard ring structure surrounding a portion of the active mask region to isolate the active region from an outer region of the mask substrate; and

a second guard ring structure having at least one fuse structure surrounding a portion of the first guard ring structure;

wherein the fuse structure is operably coupled to the active region to absorb a current from static electricity, the static electricity being accumulated by the active region to the pre-determined level and being discharged as current to the fuse structure while maintaining the active region free from damage from the static electricity.

2. The mask of claim 1 wherein the fuse structure is a plurality of conductive regions.

3. The mask of claim 1 wherein the fuse structure has a length and a thickness.

4. The mask of claim 1 wherein the fuse structure is made of a conductive material.

5. The mask of claim 1 wherein each of the fuse structures is formed on the mask substrate within a predetermined distance from a portion of the active region such that static electricity discharges to the fuse structure.

6. The mask of claim 1 wherein the fuse structure includes a plurality of conductive members, each of the conductive members including an elongated portion including a free end portion.

7. The mask of claim 1 wherein the first guard ring structure comprises a trench region free from an overlying conductive layer.

8. The mask of claim 1 wherein the first guard ring structure is continuous around the active region to electrically and physically isolate the second guard ring structure from the active region.

9. The mask of claim 1 wherein the predetermined level corresponds to a voltage no greater than 2,000,000 volts.

10. The mask of claim 1 wherein the predetermined level corresponds to a voltage no greater than 2,000,000 volts.

11. A method for manufacturing a semiconductor integrated circuit device structure comprising:

using a mask substrate, the mask substrate comprising:

an active mask region within a first portion of the mask substrate, the active region being adapted to accumulate a pre-determined level of static electricity;

a first guard ring structure surrounding a portion of the active mask region to isolate the active region from an outer region of the mask substrate; and

a second guard ring structure having at least one fuse structure surrounding a portion of the first guard ring structure; the fuse structure being operably coupled to the active region to absorb a current from static electricity, the static electricity being accumulated by the active region to the pre-determined level and being discharged as current to the fuse structure while maintaining the active region free from damage from the static electricity.

12. The method of claim 11 wherein the fuse structure is a plurality of conductive regions.

13. The method of claim 11 wherein the fuse structures is formed on the mask substrate within a predetermined distance from a portion of the active region such that static electricity discharges to the fuse structure.

14. The method of claim 11 the first guard ring structure is continuous around the active region to electrically and physically isolate the second guard ring structure from the active region.

15. The method of claim 11 wherein the fuse structure includes a plurality of conductive members, each of the conductive members including an elongated portion including a free end portion.

16. The method of claim 11 wherein each of the fuse structures is formed on the mask substrate within a predetermined distance from a portion of the active region such that static electricity discharges to the fuse structure.

17. A method for manufacturing integrated circuit devices, the method comprising:

receiving a mask in a first pod, the mask including an active region and a guard ring structure having at least one fuse structure;

transferring the mask from the first pod into a second pod within a clean room environment;

handling the mask in the clean room environment;

accumulating static electricity on the mask during the handling in the clean room environment;

discharging a portion of the static charge to the fuse on the guard ring structure of the mask while maintaining the active region of the mask free from static energy damage; and

using the mask in an operation for manufacture of semiconductor integrated circuits.

18. The method of claim 17 wherein the operation is a lithography process.

19. The method of claim 17 wherein the static energy is characterized by a voltage of 1000 volts.

20. The method of claim 17 wherein the static energy is characterized by a voltage of greater than 3000 volts.